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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEWIS, MONICA	

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2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/832,867	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10,25-38 and 51-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,25-38 and 51-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed April 9, 2007.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 2, 4-14, 25-38 and 51-64 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-10, 13, 14 and 25-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 6,909,114) in view of Shohara et al. (U.S. Patent No. 6,238,754).

In regards to claim 1, Yamazaki discloses the following:

a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (100) (For Example: See Figure 2B);

b) a channel forming region (121) (For Example: See Figure 2B);

c) an n-type impurity region (124) adjacent to the channel forming region (For Example: See Figure 2B);

d) an n-type impurity region (126) adjacent to the n-type impurity region (124) (For Example: See Figure 2B);

e) an n-type impurity region (122) adjacent to the n-type impurity region (126) (For Example: See Figure 2B);

f) a gate insulating layer (103) provided over the active layer (For Example: See Figure 2B);

g) a gate electrode (108 and 109) provided over the gate insulating layer (For Example: See Figure 2B);

h) a first conductive film (108) provided over the gate insulating layer (For Example: See Figure 2B);

i) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between and the second conductive film has a thinner width as compared with the first conductive film (For Example: See Figure 2B);

j) a protecting film (130) in contact with the gate insulating layer and the second conductive film (For Example: See Figure 12B); and

k) the first conductive film comprises one of tantalum nitride and titanium nitride and the second conductive film comprises tungsten (For Example: See Column 6 Lines 38-50).

In regards to claim 1, Yamazaki fails to disclose the following:

a) a resin film provided over the protecting film and a coloring layer provided between the protecting film and the resin film.

However, Shohara et al. ("Shohara") discloses a semiconductor device a resin film provided over the protecting film and a coloring layer (217) provided between the protecting film (216) and the resin film (230) (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a resin film provided over the protecting film and a coloring layer provided between the protecting film and the

resin film as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claim 2, Yamazaki discloses the following:

a) a driver circuit (203 and 204) having a n-channel TFT and a light emitting over a substrate (300) (For Example: See Figure 10);

b) a pixel portion having a light emitting element over the substrate (For Example: See Figure 12B);

c) a channel forming region (331) (For Example: See Figure 12B);

d) a n-type impurity region (335) adjacent to the channel forming region (For Example: See Figure 12B);

e) a n-type impurity region (337) adjacent to the n-type impurity region (335) (For Example: See Figure 12B);

f) a n-type impurity region (333) adjacent to the n-type impurity region (337) (For Example: See Figure 12B);

g) a gate insulating layer (305) provided over the active layer (For Example: See Figure 12B);

h) a gate electrode (370) provided over the gate insulating layer (For Example: See Figure 12B);

i) a first conductive film (371) provided over the gate insulating layer (For Example: See Figure 12B);

j) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between and the second conductive film has a thinner width as compared with the first conductive film (For Example: See Figure 12B); and

k) a pixel portion having a light emitting element over the substrate (100) (For Example: See Figure 12B).

In regards to claim 2, Yamazaki fails to disclose the following:

a) a resin film provided over the protecting film and a coloring layer provided between the protecting film and the resin film.

However, Shohara discloses a semiconductor device a resin film provided over the protecting film and a coloring layer provided between the protecting film and the resin film (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a resin film provided over the protecting film and a coloring layer provided between the protecting film and the resin film as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 4, 27 and 28, Yamazaki discloses the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride and the second conductive film comprises tungsten (For Example: See Column 6 Lines 38-50).

In regards to claims 5, 6, 29 and 30, Yamazaki discloses the following:

a) the first conductive film comprises tungsten and the second conductive film comprises aluminum (For Example: See Column 6 Lines 38-50).

In regards to claims 7, 8, 31 and 32, Yamazaki discloses the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from $1x10^{20}$ to $1x10^{21}$ atoms/cm^3, the n-type doped region includes an n-type impurity element in concentrations of from $2x10^{16}$ to $5x10^{19}$atoms/cm^3, and the n-type doped region includes an n-type impurity element in concentrations from $1x10^{16}$ to $5x10^{19}$atoms/cm^3 (For Example: See Column 9 Lines 45-67).

Additionally, the applicant has not established the critical nature of concentrations from $1x10^{20}$ to $1x10^{21}$ atoms/cm^3, $2x10^{16}$ to $5x10^{19}$atoms/cm^3, and $1x10^{16}$ to $5x10^{19}$atoms/cm^3. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claims 9 and 10, Yamazaki fails to disclose the following:

a) the gate electrode is covered by a protection film comprising at least one of a silicon nitride film and a silicon oxynitride films.

However, Shohara discloses a semiconductor device where the gate electrode is covered by a protection film comprising at least one of a silicon nitride film and a silicon oxynitride films (For Example: See Column 13 Lines 7-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate electrode covered by a protection film comprising at least one of a silicon nitride film and a silicon oxynitride films as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 13, 14, 37 and 38, Yamazaki discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Figure 32A).

In regards to claims 9 and 10, Yamazaki discloses the following:

a) the gate electrode is covered by an insulating film (307) comprising at least one of a silicon nitride film and a silicon oxynitride films are laminated (For Example: See Column 17 Lines 29-32).

In regards to claim 25, Yamazaki discloses the following:

a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (100) (For Example: See Figure 2B);

b) a channel forming region (121) (For Example: See Figure 2B);

c) an n-type impurity region (124) adjacent to the channel forming region (For Example: See Figure 2B);

d) an n-type impurity region (126) adjacent to the n-type impurity region (124) (For Example: See Figure 2B);

e) an n-type impurity region (122) adjacent to the n-type impurity region (126) (For Example: See Figure 2B);

f) a gate insulating layer (103) provided over the active layer (For Example: See Figure 2B);

g) a gate electrode (108 and 109) provided over the gate insulating layer (For Example: See Figure 2B);

h) a first conductive film (108) provided over the gate insulating layer (For Example: See Figure 2B); and

i) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between and the second conductive film has a thinner width as compared with the first conductive film (For Example: See Figure 2B).

In regards to claim 25, Yamazaki fails to disclose the following:

a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer (217) over the gate electrode (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claim 26, Yamazaki discloses the following:

a) a driver circuit (203 and 204) having a n-channel TFT and a light emitting over a substrate (300) (For Example: See Figure 10);

b) a channel forming region (331) (For Example: See Figure 12B);

c) a n-type impurity region (335) adjacent to the channel forming region (For Example: See Figure 12B);

d) a n-type impurity region (337) adjacent to the n-type impurity region (335) (For Example: See Figure 12B);

e) a n-type impurity region (333) adjacent to the n-type impurity region (337) (For Example: See Figure 12B);

f) a gate insulating layer (305) provided over the active layer (For Example: See Figure 12B);

g) a gate electrode (370) provided over the gate insulating layer (For Example: See Figure 12B);

h) a first conductive film (371) provided over the gate insulating layer (For Example: See Figure 12B); and

i) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between and the second conductive film has a thinner width as compared with the first conductive film (For Example: See Figure 12B).

In regards to claim 26, Yamazaki fails to disclose the following:

a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer (217) over the gate electrode (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 33 and 34, Yamazaki discloses the following:

a) the gate electrode is covered by an insulating film (307) comprising at least one of a silicon nitride film and a silicon oxynitride films are laminated (For Example: See Column 17 Lines 29-32).

In regards to claims 35 and 36, Yamazaki fails to disclose the following:

a) a coloring layer provided between the resin film and the silicon nitride.

However, Shohara discloses a semiconductor device that has a coloring layer (217) provided between the resin film (230) and the silicon nitride (216) (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided between the resin film and the silicon nitride as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

6. Claims 51-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 6,909,114) in view of Shohara et al. (U.S. Patent No. 6,238,754) and Takemura et al. (U.S. Patent No. 6,835,607).

In regards to claim 51, Yamazaki discloses the following:

a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (100) (For Example: See Figure 2B);

b) a channel forming region (121) (For Example: See Figure 2B);

c) an n-type impurity region (124) adjacent to the channel forming region (For Example: See Figure 2B);

d) an n-type impurity region (126) adjacent to the n-type impurity region (124) (For Example: See Figure 2B);

e) an n-type impurity region (122) adjacent to the n-type impurity region (126) (For Example: See Figure 2B);

f) a gate insulating layer (103) provided over the active layer (For Example: See Figure 2B);

g) a gate electrode (108 and 109) provided over the gate insulating layer (For Example: See Figure 2B);

h) a first conductive film (108) provided over the gate insulating layer (For Example: See Figure 2B); and

i) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 2B).

In regards to claim 51, Yamazaki fails to disclose the following:

a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer (217) over the gate electrode (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

b) the gate insulating layer has a greater thickness over the channel forming region than over the n-type impurity region.

However, Takemura et al. ("Takemura") discloses a gate insulating layer (6) that has a greater thickness over the channel forming region (3) than over the impurity region (2) (For Example: See Figure 2d). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate insulating layer that has a greater thickness over the channel

forming region than over the impurity region as disclosed in Takemura because it aids in protecting the reliability of the film (For Example: See Column 4 Lines 3-6).

Additionally, since Yamazaki and Takemura are both from the same field of endeavor, the purpose disclosed by Takemura would have been recognized in the pertinent art of Yamazaki.

In regards to claim 52, Yamazaki discloses the following:

a) a driver circuit (203 and 204) having a n-channel TFT and a light emitting over a substrate (300) (For Example: See Figure 10);

b) a pixel portion having a light emitting element over the substrate (For Example: See Figure 12B);

c) a channel forming region (331) (For Example: See Figure 12B);

d) a n-type impurity region (335) adjacent to the channel forming region (For Example: See Figure 12B);

e) a n-type impurity region (337) adjacent to the n-type impurity region (335) (For Example: See Figure 12B);

f) a n-type impurity region (333) adjacent to the n-type impurity region (337) (For Example: See Figure 12B);

g) a gate insulating layer (305) provided over the active layer (For Example: See Figure 12B);

h) a gate electrode (370) provided over the gate insulating layer (For Example: See Figure 12B);

i) a first conductive film (371) provided over the gate insulating layer (For Example: See Figure 12B);

j) a second conductive film (109) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 12B).

In regards to claim 52, Yamazaki fails to disclose the following:

a) a coloring layer over the gate electrode.

However, Shohara discloses a coloring layer (217) over the gate electrode (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer over the gate electrode as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

b) the gate insulating layer has a greater thickness over the channel forming region than over the n-type impurity region.

However, Takemura discloses a gate insulating layer (6) that has a greater thickness over the channel forming region (3) than over the impurity region (2) (For Example: See Figure 2d). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a gate insulating layer that has a greater thickness over the channel forming region than over the impurity region as disclosed in Takemura because it aids in protecting the reliability of the film (For Example: See Column 4 Lines 3-6).

Additionally, since Yamazaki and Takemura are both from the same field of endeavor, the purpose disclosed by Takemura would have been recognized in the pertinent art of Yamazaki.

In regards to claims 53 and 54, Yamazaki discloses the following:

a) the first conductive film comprises one of tantalum nitride and titanium nitride and the second conductive film comprises tungsten (For Example: See Column 6 Lines 38-50).

In regards to claims 55 and 56, Yamazaki discloses the following:

a) the first conductive film comprises tungsten and the second conductive film comprises aluminum (For Example: See Column 6 Lines 38-50).

In regards to claims 57 and 58, Yamazaki discloses the following:

a) the n-type impurity region includes an n-type impurity element in concentrations from $1x10^{20}$ to $1x10^{21}$ atoms/cm^3, the n-type doped region includes an n-type impurity element in concentrations of from $2x10^{16}$ to $5x10^{19}$atoms/cm^3, and the n-type doped region includes an n-type impurity element in concentrations from $1x10^{16}$ to $5x10^{19}$atoms/cm^3 (For Example: See Column 9 Lines 45-67).

Additionally, the applicant has not established the critical nature of concentrations from $1x10^{20}$ to $1x10^{21}$ atoms/cm^3, $2x10^{16}$ to $5x10^{19}$atoms/cm^3, and $1x10^{16}$ to $5x10^{19}$atoms/cm^3. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claims 59 and 60, Yamazaki discloses the following:

a) the gate electrode is covered by an insulating film (307) comprising at least one of a silicon nitride film and a silicon oxynitride films are laminated (For Example: See Column 17 Lines 29-32).

In regards to claims 61 and 62, Yamazaki fails to disclose the following:

a) a coloring layer provided between the resin film and the silicon nitride.

However, Shohara discloses a semiconductor device that has a coloring layer (217) provided between the resin film (230) and the silicon nitride (216) (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamazaki to include a coloring layer provided between the resin film and the silicon nitride as disclosed in Shohara because it aids in providing good display characteristics (For Example: See Column 13 Lines 7-35).

Additionally, since Yamazaki and Shohara are both from the same field of endeavor, the purpose disclosed by Shohara would have been recognized in the pertinent art of Yamazaki.

In regards to claims 63 and 64, Yamazaki discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Figure 32A).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML
July 8, 2007

MONICA LEWIS
PRIMARY PATENT EXAMINER